HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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11-29-05

PATENT APPLICATION AP/IFW

ATTORNEY DOCKET NO. 10002827.2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kent A. Dickey et al. **Confirmation No.:** 1746

Application No.: 10/664,763 **Examiner:** M. C. Maskulinski

Filing Date: 09-17-2003 **Group Art Unit:** 2113

Title: METHOD FOR ALLOWING DISTRIBUTED HIGH PERFORMANCE COHERENT MEMORY WITH FULL ERROR CONTAINMENT

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **09-26-05**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV568265804US, in an envelope addressed to: MS Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450
Date of Deposit: **November 28, 2005**

Number of pages:

Typed Name: **Susan Bloomfield**

Signature: Susan Bloomfield

Respectfully submitted,

Kent A. Dickey et al.

By R Ross Viguet

R. Ross Viguet

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Docket No.: 10002827-2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kent A. Dickey et al.

Application No.: 10/664,763 | Confirmation No.: 1746

Filed: September 17, 2003 | Art Unit: 2113

For: METHOD FOR ALLOWING DISTRIBUTED HIGH PERFORMANCE COHERENT MEMORY WITH FULL ERROR CONTAINMENT | Appellee: M. C. Maskulinski

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sirs:

As required under 37 C.F.R. § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on September 26, 2005, and is in furtherance of said Notice of Appeal.

The fees required under 37 C.F.R. § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Parkard Development Company, L.P., a Texas Limited Partnership having its principle place of business in Houston, Texas.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 20 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1-20

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 21-40

4. Claims allowed: None

5. Claims rejected: 21-39

C. Claims On Appeal

Claims 21-40 are on appeal.

IV. STATUS OF AMENDMENTS

A Final Office Action (hereinafter the "Final Action") was mailed on August 12, 2005. The Appellant did not file an Amendment After Final Rejection; as such, the claims are pending as submitted in the Response filed on June 16, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to claim 21, the method for providing a distributed high performance coherent memory with error containment comprises the steps of: reading an error indication included in a data packet, reflective of a current state of a unit [pg. 10, line 25-pg. 11, line 1], determining if said current state of said unit is in error mode [pg. 11, line 25- pg. 12, line 3; figure 4, 90-112], permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode [pg. 11, lines 24-26], driving an error indicator to a subject processor if said current state of unit is in error mode [pg. 12, lines 6-8; figure 6, 144, 152], and ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode [pg. 12, lines 18-21; figure 8].

According to claim 32, the distributed high performance coherent memory module with error containment comprises: a reading module for reading an error indication included in a data packet reflective of a current state of a unit [pg. 10, line 25-pg. 11, line 1], a determination module for determining if said state of a unit is in error mode [pg. 11, line 25-pg. 12, line 3; figure 4, 90-112], a permission module for permitting a set of network traffic to operate in a normal state if said state of said unit is not in error mode [pg. 11, lines 24-26], a driving module for driving an error indicator to a subject processor if said state of said unit is in error mode [pg. 12, lines 6-8; figure 6, 144, 152], a blocking module for ensuring that a set of corrupt traffic does not reach I/O devices if said current state of unit is in error mode [pg. 12, lines 18-21; figure 8], and a second reading module for ensuring that each member of a group of connected units reads said error indication included in said data packet, if said state of said unit is in error mode [pg. 10, line 24-pg. 11, line 4].

According to claim 39, the system for error containment comprises: a means for transporting error indications together with data which is in error [pg. 8, lines 19-22; figure 2, 30], and a means at each device to which such error data is directed and controlled in part by said error indicators for containing within said device said error data [pg. 10, lines 13-18].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 21, 24-31, and 39 are properly rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,295,585 to Gillett, Jr. et al. (hereinafter "Gillett").

B. Whether claims 22, 23, and 32-37 are properly rejected under the judicially created doctrine of obviousness-type double patenting.

VII. ARGUMENT

Claims 21, 24-31, and 39 are rejected under 35 U.S.C. § 102(e) as being anticipated by Gillett Jr., et al. ('585, hereinafter Gillett).

It is well settled that to anticipate a claim, the reference must teach every element of the claim. Moreover, in order for a prior art reference to be anticipatory under 35 U.S.C. §

102 with respect to a claim, "[t]he elements must be arranged as required by the claim," *see In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). Furthermore, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," *see Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989).

Claim 21 defines a method for providing a distributed high performance coherent memory with error containment that includes reading an error indication included in a data packet, reflective of a current state of a unit. Gillett does not disclose at least this limitation. In the Final Action, the Appellee asserts that Gillett discloses the STAE and SRAE bits which reads on the limitations of claim 21. Gillet, at column 8, line 35 to column 9, line 2, teaches that the STAE bit is not part of a packet, but rather is part of a page control table (i.e. the transmit page control table). Similarly, the SRAE bits also are not part of a packet, but also are part of a page control table (i.e. the receive page control table), see Table 1. Thus, Gillett does not teach all of the claimed limitations. Therefore, the Appellant respectfully asserts that for at least the reasons set forth above, claim 21 is patentable over the 35 U.S.C. § 102 rejection of record.

Claim 32 defines a distributed high performance coherent memory module with error containment that includes a reading module for reading an error indication included in a data packet reflective of a current state of a unit. Gillett does not disclose at least this limitation. In the Final Action, the Appellee asserts that Gillett discloses the STAE and SRAE bits which reads on the limitations of claim 21. Gillet, at column 8, line 35 to column 9, line 2, teaches that the STAE bit is not part of a packet, but rather is part of a page control table (i.e. the transmit page control table). Similarly, the SRAE bits also are not part of a packet, but also are part of a page control table (i.e. the receive page control table), see Table 1. Thus, Gillett does not teach all of the claimed limitations. Therefore, the Appellant respectfully asserts that for at least the reasons set forth above, claim 21 is patentable over the 35 U.S.C. § 102 rejection of record.

Claim 39 defines a system for error containment comprising means for transporting error indications together with data which is in error. Gillett does not disclose at least this limitation. The Office Action states that Gillett discloses the STAE and SRAE bits which

reads on the limitations of claim 19. Column 8, line 35 to column 9, line 2, Gillett teaches that the STAE bit is not part of a packet, but rather is part of a page control table (i.e. the transmit page control table). Similarly, the SRAE bits also are not part of a packet, but also are part of a page control table (i.e. the receive page control table). Thus, Gillett does not teach all of the claimed limitations. Therefore, the Appellant respectfully asserts that for the above reasons claim 39 is patentable over the 35 U.S.C. § 102 rejection of record.

Claims 24-31 depend directly from base claim 21, and thus inherits all limitations of claim 1. Each of claims 24-31 sets forth features and limitations not recited by Gillett. Thus, the Appellant respectfully asserts that for the above reasons claims 24-31 are patentable over the 35 U.S.C. § 102 rejection of record.

Whether claims 22, 23, and 32-37 are properly rejected under the judicially created doctrine of obviousness-type double patenting. The Appellant propose filing a terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) if such is still necessary after the Board renders its decision in this pending case.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Appellant on June 16, 2005.

IX. EVIDENCE

No evidence pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Appellee is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no such Appendix is included.

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Date of Deposit: November 28, 2005

Typed Name: Susan Bloomfield

Signature: Susan Bloomfield

Respectfully submitted,

By _____

R. Ross Viguet
Attorney/Agent for Applicant(s)
Reg. No.: 42,203

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/664,763

21. (Previously Presented) A method for providing a distributed high performance coherent memory with error containment, comprising the steps of:

reading an error indication included in a data packet, reflective of a current state of a unit;

determining if said current state of said unit is in error mode;

permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode;

driving an error indicator to a subject processor if said current state of unit is in error mode; and

ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode.

22. (Previously Presented) The method of claim 21 further including the step of:

ensuring that each member of a group of connected units, reads said error indication included in said data packet, if said current state of a unit is in error mode.

23. (Previously Presented) The method of claim 22 further including the step of:

ensuring that each member of said group of connected units having at least one connected unit passes said error indication included in said data packet if said current state of a unit is in error mode to a next member of said group of connected units.

24. (Previously Presented) The method of claim 21 wherein said error indication in said data packet is in the form of an error bit.

25. (Previously Presented) The method of claim 21 wherein said error indication in said data packet contained within a header of said data packet.

26. (Previously Presented) The method of claim 21 further comprising the step of:

implementing a recovery routine by said subject processor.

27. (Previously Presented) The method of claim 21 wherein said reading step includes reading said error indication from an error bit.

28. (Previously Presented) The method of claim 21 further comprising the step of: implementing a software recovery routine to clear said error mode.

29. (Previously Presented) The method of claim 21, further comprising the step of:

setting a shared memory error bit to be included in said data packet as representative of a presence of an error in a shared memory area.

30. (Previously Presented) The method of claim 29, wherein said error bit is provided as a fatal error bit.

31. (Previously Presented) The method of claim 29, wherein said error bit is provided as a shared memory bit, and wherein said unit comprises a shared memory area.

32. (Previously Presented) A distributed high performance coherent memory module with error containment, comprising:

a reading module for reading an error indication included in a data packet reflective of a current state of a unit;

a determination module for determining if said state of a unit is in error mode;

a permission module for permitting a set of network traffic to operate in a normal state if said state of said unit is not in error mode;

a driving module for driving an error indicator to a subject processor if said state of said unit is in error mode;

a blocking module for ensuring that a set of corrupt traffic does not reach I/O devices if said current state of unit is in error mode; and

a second reading module for ensuring that each member of a group of connected units reads said error indication included in said data packet, if said state of said unit is in error mode.

33. (Previously Presented) The module of claim 32 further comprising:

a passing module for ensuring that each member of a group of connected units passes said error indication included in said data packet, if said current state of a unit is in error mode, to a next unit member of group of connected units having at least one connected unit.

34. (Previously Presented) The module of claim 32 further comprising an error indication module for providing an error indication to be included in said data packet reflective of the current state of a unit.

35 (Previously Presented) The module of claim 32 further comprising:

a processor recovery module for implementing a recovery routine by said subject processor.

36. (Previously Presented) The module of claim 32 further comprising:

a unit recovery module for implementing a software recovery routine to clear said error mode from said unit.

37. (Previously Presented) The module of claim 32 further comprising:

a shared memory error module for setting a shared memory error bit to be included in said data packet for representing the presence of an error in a shared memory area.

38. (Previously Presented) The error indication module of claim 32 further comprising:

a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit; and

means for moving said error indication coextensive only with errors in particular data.

39. (Previously Presented) A system for error containment, said system comprising:

means for transporting error indications together with data which is in error; and

means at each device to which such error data is directed and controlled in part by said error indicators for containing within said device said error data.

40. (Previously Presented) A system for error containment as set forth in claim 39 further including:

means for propagating said error indications to next ones of said devices to which said error data must be delivered, said propagating occurring concurrently with error data delivery.